Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Please amend the claims as follows:

Claims 1-18 (Cancelled).

19. (Previously Presented) A device comprising:

first circuitry to generate a packet ~~header~~ based on ~~payload~~ header data received from a micro-engine [[or]] and packet header data from a memory controller, the first circuitry comprising:

second circuitry to receive packet data from the memory controller ~~or the micro-engine~~, and to store the packet data in first-in first-out (FIFO) circuitry; and

third circuitry to track a start lane in the FIFO circuitry indicating a start of free space in the FIFO circuitry, and to determine a starting lane for packet payload such that alignment of payload data matches the start lane in the FIFO circuitry.

20. (Previously Presented) The device of claim 19, wherein the second circuitry comprises:

logic to synchronize receipt of the packet header from the micro-engine and the packet payload from the memory controller, to store the packet header in the FIFO circuitry, and

to transfer the packet header and packet payload data from the FIFO circuitry to a destination specified in the packet header.

21. (New) The device of claim 19, wherein the micro engine is a direct memory access (DMA) controller send queue to transmit requests and receive responses.

22. (New) The device of claim 19, wherein the micro engine is a direct memory access (DMA) controller receive queue to transmit response and receive requests.

23. (New) A method comprising:

receiving packet data from a memory controller;

storing the packet date in first-in first-out (FIFO) queue;

tracking a start lane in the FIFO queue indicating a start of free space in the FIFO queue;

determining a starting lane for packet payload such that alignment of payload data matches the start lane in the FIFO queue; and

generating a packet header based on the payload data.